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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/724,996	12/01/2003	Stefan Auracher	03-0352 1496.00327	3153

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EXAMINER	
SIEK, VUTHE	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 08/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/724,996	AURACHER ET AL.	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/1/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/724,996 filed on 12/1/2003. Claims 1-24 remain pending in the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Solomon et al. (6,446,248).

4. As to claims 1, 5 and 21, Solomon et al. teach methods for designing an integrated circuit (IC), where the IC is first created by placing and routing standard cells of the IC, then empty spaces unused by the standard cells are extracted. The extracted unused areas are used (re-used) by inserting clusters of metal-programmable transistors by an area-based placement/routing tool to "ponds" of gates (PODs) (re-used cells). When design changes are desired after formation of the IC, the metal-programmable transistors (re-used cells) are programmed to form desired spares cells (re-used cells) to implement the desired design changes by making changes to the upper layer metals for the IC (macro cell) (see abstract, summary, Figs. 2-5 and its description).

5. As to claim 14, remarks set forth in rejecting claim 1, 5 and 21 equally apply in rejection of claim 14. In addition, Solomon et al. teach base cells are inserted to form PODs cells in different parts of the IC design layout to accomplish design changes when needed (col. 7). The base cells must be buffers, inverters, repeaters or other logic gates because they are usually used in IC design changes. The inserted base cells are metal-programmable transistors to implement the IC design changes by making changes to the upper layer metals for to the IC design layout. The inserted base cells are located close proximity to standard cells to facilitate interconnect there between by placement/routing tool. Thus this would suggest the claimed limitation of interconnection.

6. As to claims 2-4, 6-8 and 16-17, Solomon et al. teach base cells are inserted to form PODs cells in different part of the IC design layout to accomplish design changes (col. 7). The base cells must be either buffers, inverters, repeaters or other logic gates because they are usually used to IC design changes. In addition, the inserted base cells are metal-programmable transistors to implement the design changes by making changes to the upper layer metals for to the IC design layout. This is done by a user definable interconnection layer of the IC layout.

7. As to claim 15, Solomon et al. teach base cells are inserted to form PODs cells in different parts of the IC design layout to accomplish design changes when needed (col. 7). The base cells are used in IC design changes by forming interconnection as necessary to placement/routing tool. The inserted base cells are metal-programmable transistors to implement the IC design changes by making changes to the upper layer

metals for to the IC design layout. The inserted base cells are located close proximity to standard cells to facilitate interconnect there between by placement/routing tool. Thus this would suggest the claimed limitation of interconnection.

8. As to claim 18, Solomon et al. teach base cells are inserted to form PODs cells in different parts of the IC design layout to accomplish design changes when needed (col. 7). The base cells (first and second repeater cells) must be buffers, inverters, repeaters or other logic gates because they are usually used in IC design changes in order to fix a delay problem. The inserted base cells are metal-programmable transistors to implement the IC design changes by making changes to the upper layer metals for to the IC design layout. The inserted base cells are located close proximity to standard cells to facilitate interconnect there between by placement/routing tool. Thus this would suggest the claimed limitation of interconnection.

9. As to claims 19-20, the first and second repeater cells (base cells inserted) must be the same circuit type (inverter circuit cells) when they are used as drivers or buffer. This is a common practice in IC design changes.

10. As to claims 9 and 22, Solomon et al. teach the inserted base cells are used in IC design changes. Thus, the IC design changes are generated by a plurality of design representations of IC design layout (macro) in which different numbers of inserted base cells (reusable sub-circuit cells) because the inserted base cells are programmable cells.

11. As to claims 10 and 23, Solomon et al. teach the inserted base cells (reusable cells) are used in IC design changes. Thus, when there are no IC design changes are generated, none of the inserted base cells are reusable.

12. As to claims 11-13 and 24, Solomon et al. teach base cells are inserted to form PODs cells in different parts of the IC design layout to accomplish design changes when needed (col. 7). The base cells (first and second repeater cells) must be buffers, inverters, repeaters or other logic gates because they are usually used in IC design changes in order to fix a delay problem (parameter). The inserted base cells are metal-programmable transistors to implement the IC design changes by making changes to the upper layer metals for to the IC design layout. The inserted base cells are located close proximity to standard cells to facilitate interconnect there between by placement/routing tool. In order to fully use the reusable cells, a designer must insert certain number of base cells in order to eliminate waste spaces in IC design layout.

13. Claims 1-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Wong et al. (6,255,845).

14. As to claims 1, 5, 14 and 21, Wong et al. teach a method for implementing logic enhancements of an IC design (macro) that includes a pre-defined chip logic and a plurality of spare cells, where the spare cells (invertors, buffers, repeaters) includes logic gates, configurable building block circuit and inverters for interconnection when needed (see abstract, summary, Fig. 1-9 and its description). Fig. 5 shows the spare cell 151 in spare state (not used), where inputs and outputs are left open (unconnected). In this condition, none of the circuits (spare cells) within the cell are in

use. When needed, the inputs and outputs are interconnected appropriately to realize specific logic a function as required to form an IC design based on design changes. In this condition, the spare cells are in use or they are reusable by making connections of inputs and outputs of the spare cells to certain layers of semiconductor device to be built to obtain specific logic function. Fig. 1-2 show examples of connections. The connection as recited in claim 14 would be realized using placement and routing tool.

15. As to claims 2-4, 6-13, 15-20 and 22-24, Wong et al. teach using spare cells to implement a logic function from a base IC design by forming connections of inputs and outputs of the spare cells to other standard cells using metal layers by an automatic placement and routing tool as specified by a designer (see Fig. 1-2). The spare cells include inverters (repeater cells), buffers, logic gates and configurable building block circuit. Since the spare cells are used to implement a plurality of IC designs, a plurality of design representations of IC design (macro) must generated using different number of spare cells. When the cells are in spare state, they are not in used meaning that none of the circuits within the cell are in use (col. 8). When they in use or needed or reused (reuse permission, the spare cells are fully reusable), the inputs and outputs of appropriate spare cells are interconnected with other standard cells in order to form a logic function as required as instructed by a designer. The connections are performed (connection paths including first, second, third connection paths) by placement and routing tool as instructed by a designer. This would suggest generating a parameter defining a reuse permission for the reusable sub-circuit cell.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906. The examiner can normally be reached on Increase Flextime.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek

VUTHE SIEK
PRIMARY EXAMINER